WORKSHOP 4

A half-day workshop in Advanced VLSI Design

Date : 11 December 2015 (Friday)
Time : 9:30 a.m. – 1:00 p.m.
Venue : Room CF504, Department of Electronic and Information Engineering, The Hong Kong Polytechnic University, Hung Hom, Hong Kong

Topic : **High Level Synthesis**
Speaker : **Dr Benjamin Carrion Schafer**, Assistant Professor, PolyU EIE

Abstract

The International Technology Roadmap for Semiconductors (ITRS) suggests that by 2020 a 10x productivity increase for designing complex System on Chips (SoCs) is needed. Two main factors are predicted to help achieving this goal. The first is the re-use of components. ITRS estimates that around 90% of the SoCs will be composed of re-used components. Secondly is the use of new design methodologies to raise the level of abstraction i.e. High-Level Synthesis (HLS), also called C-based design.

C-Based design has many advantages compared to traditional RTL design. First, it increases the design productivity, which allows design teams to meet the increasingly stringent time-to-market requirements. Second, the ability to create smaller designs compared to hand-coded RTL due to its ability to maximize resource sharing. Lastly, the possibility of generating a set of micro-architectures with different area vs. performance trade-offs without having to modify the original behavioral description, also called Design Space Exploration (DSE) are some of them.

This workshop focuses on C-based design based on High-Level Synthesis and how to integrate this new design methodology into a traditional RTL-based VLSI design methodology. This includes how to verify these designs and co-verify legacy RTL blocks with newly developed C-based design processes.

Biography

Dr Benjamin Carrion Schafer completed his Ph.D. at the University of Birmingham, U.K., in 2002. He then worked in the Computer Science Department at the University of California Los Angeles (UCLA) as a Postdoctoral Researcher from 2003 to 2004 and then joined the School of Electronic Engineering and Computer Science at Seoul National University, Korea, as a Visiting Research Scholar from 2005 to 2007. From 2007 until September 2012, he was a researcher at System IP Core Department, Central R&D Centre, NEC Corporation, Kawasaki, Japan. Since 2012, he works as an Assistant Professor at the Department of Electronic and Information Engineering (EIE) at The Hong Kong Polytechnic University, where he established the Design Automation and Reconfigurable Computing Laboratory (DARClab).

Dr Carrion Schafer has been engaged in the research and development of VLSI systems, reconfigurable computing, thermal-aware VLSI design and High Level Synthesis (HLS). He has over 30 publications as the first author in international scientific journals, conferences and books. He served on the TPC of most EDA and FPGA conferences including CASES, RECONFIG, FPL, DAC, ASP-DAC and ESLSyn. He was also a member of Accellera's SystemC synthesizable user group committee, leading the effort to standardize a synthesizable subset of SystemC. He holds an MBA from McGill University.